In the Claims:

Please amend Claims 1 as follows (the changes in these Claims are shown with strikethrough for deleted matter and <u>underlines</u> for added matter). A complete listing of the claims proper claim identifiers is set forth below.

- 1. (Currently amended) A method of processing data in a bi-directional processing device, the method comprising:
- (a) receiving said data by a first processor from a bi-directional interface, said first processor operative to perform a first task on said data thereby resulting in processed data;
- (b) storing said processed data in a shared memory by said first processor, said shared memory comprising first and second banks, wherein one of said first and second banks is accessible to said first processor and the other of said first and second banks is accessible to a second processor;
- (c) mirroring said processed data stored by said first processor in said one of said first and second banks to the other of said first and second banks;
- (e)(d) retrieving said processed data from <u>said other of said first and second banks of</u> said shared memory by a <u>said</u> second processor operative to perform a second task on said <u>processed</u> data thereby resulting in secondarily processed data; and
- (d)(e) transmitting, selectively, said <u>secondarily</u> processed data to said bi-directional interface from said second processor.
- 2. (Cancelled)
- 3. (Original) The method of Claim 1, wherein said first task comprises at least one of inspection and analysis.
- 4. (Currently amended) The method of Claim 1, wherein said second task comprises taking an action on said processed data.
- 5. (Currently amended) The method Claim 4, wherein said taking an action comprises at least one of deleting, modifying and transmitting said <u>processed</u> data.
- 6. (Currently amended) The method of Claim 1, wherein each of said first and second

processors are is characterized by a bi-directional bandwidth, said method further comprising utilizing substantially all of said bi-directional bandwidth for uni-directional data flow.

- 7. (Original) The method of Claim 1, wherein said storing further comprises storing said processed data such that said second processor is unaware of how said processed data was stored in said shared memory.
- 8. (Currently amended) The method of Claim 1, wherein said method further comprises using first and second processors which comprise network processors.
- 9. (Original) The method of Claim 1, wherein said transmitting is further based on a result of said second task.
- 10. (Original) A bi-directional data processor comprising:

a first processor coupled with a bi-directional interface and operative to receive data from said bi-directional interface and perform a first task on said data thereby resulting in processed data;

a shared memory coupled with said first processor, said shared memory comprising first and second banks, wherein one of said first and second banks is accessible to said first processor, wherein said first processor is further operative to store said processed data in said one of said of said first and second banks of said shared memory; and

mirroring logic coupled with said first processor and said first and second banks and operative to mirror said processed data stored by said first processor in said one of said first and second banks to the other of said first and second banks; and

a second processor coupled with said shared memory and said bi-directional interface, said second processor operative to retrieve said stored processed data from said other of said first and second banks of said shared memory, perform a second task on said stored processed data thereby resulting in secondarily processed data and selectively transmit said secondarily processed data back to said bi-directional interface.

- 11. (Cancelled)
- 12. (Original) The bi-directional data processor of Claim 10, wherein said first task comprises at least one of inspection and analysis.

- 13. (Currently amended) The bi-directional data processor of Claim 10, wherein said second task comprises taking an action on said stored processed data.
- 14. (Original) The bi-directional data processor Claim 13, wherein said taking an action comprises at least one of deleting, modifying and transmitting said data.
- 15. (Original) The bi-directional data processor of Claim 10, wherein each of said first and second processors are characterized by a bi-directional bandwidth, substantially all of said bi-directional bandwidth being utilized for uni-directional data flow.
- 16. (Original) The bi-directional data processor of Claim 10, wherein said second processor is unaware of how said processed data was stored in said shared memory.
- 17. (Currently amended) The bi-directional data processor of Claim 10, wherein said first and second processors comprises comprise network processors.
- 18. (Currently amended) The bi-directional data processor of Claim 10, wherein said the selective transmission by said second processor is further based on a result of said second task.
- 19. (Currently amended) An apparatus for processing a bi-directional dataflow comprising: first processor means for receiving data from a bi-directional interface and performing a first task on said data thereby resulting in processed data;

shared memory means coupled with said first processor, said shared memory comprising first and second banks, wherein one of said first and second banks is accessible by said first processor means, wherein said first processor is further operative to store said processed data in said one of said first and second banks of said shared memory means; and

memory mirroring means coupled with said first processor and said first and second banks and operative to mirror said processed data stored by said first processor in said one of said first and second banks to the other of said first and second banks; and

second processor means coupled with said shared memory <u>means</u> and operative to retrieve said stored processed data from <u>said other of said first and second banks of</u> said shared memory <u>means</u>, perform a second task on said <u>processed</u> data, thereby resulting in <u>secondarily</u> <u>processed data</u>, and selectively transmit said <u>secondarily processed</u> data back to said bidirectional interface.